

Cover Sheet	1
Block Diagram/Clock Map/Power Map	2-4
Intel LGA775 CPU	5-7
Intel Lakeport - MCH	8-11
Intel ICH7 - PCI & DMI & CPU & IRQ	12
Intel ICH7 - LPC & ATA & USB & GPIO	13
Intel ICH7 - POWER	14
Clock - RTM 876-665	15
LPC I/O - Fintek 71882FG	16
LAN REALTEK RTL8111C/8101E	17
DDR II DIMM A	18
DDR II DIMM B	19
DDR II VTT Decoupling	20
Azalia - ALC888	21
PCI EXPRESS X16 Slot	22
PCI Slot 1 & 2	23
ATA33/66/100 IDE & SATA Connectors	24
USB Connectors	25
ATX Connetcor & Front Panel	26
VGA Connector	27
UPI ACPI CONTROLLER	28
GMCH VCORE	29
PWM-ST L6703TR	30

MS-7313

Version 1.0

CPU:

Intel Prescott (L2=2MB) - 3.4G & Above
 Intel Cendar Mill (65nm) - 3.73G & Above
 Intel Smithfield (90nm Dual core)
 Intel Conroe (65W Dual core)

System Chipset:

Intel Lakeport - MCH (North Bridge)
 Intel ICH7R (South Bridge)

On Board Chipset:

BIOS -- SPI
 HD -- ALC888
 LPC Super I/O -- F71882FG
 LAN-- REALTEK RTL8111C Co-lay RTL8101E
 CLOCK -- RTM876-665

Main Memory:

DDR II *2 (Max 4GB)

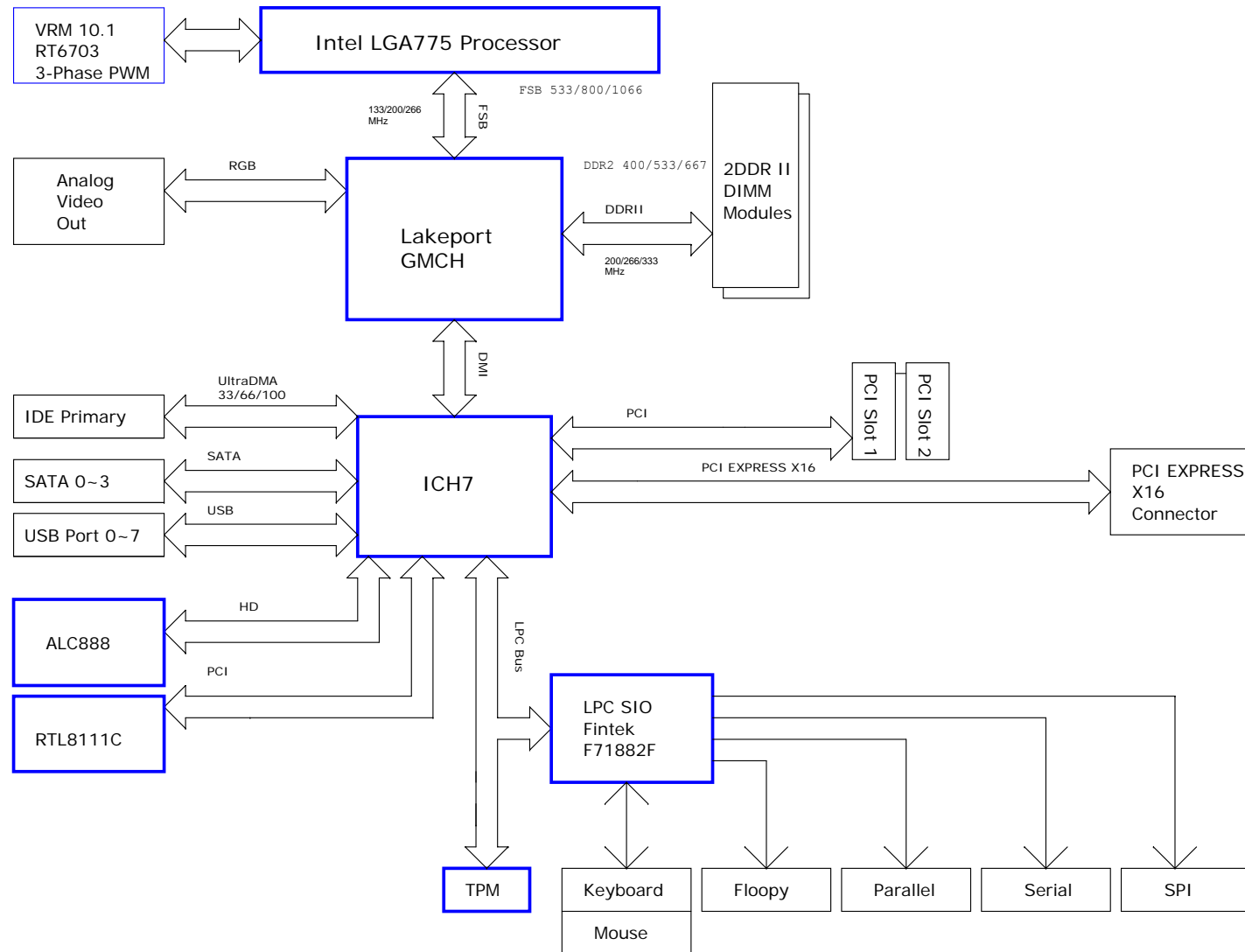
Expansion Slots:

PCI2.3 SLOT * 2
 PCI EXPRESS X16 SLOT

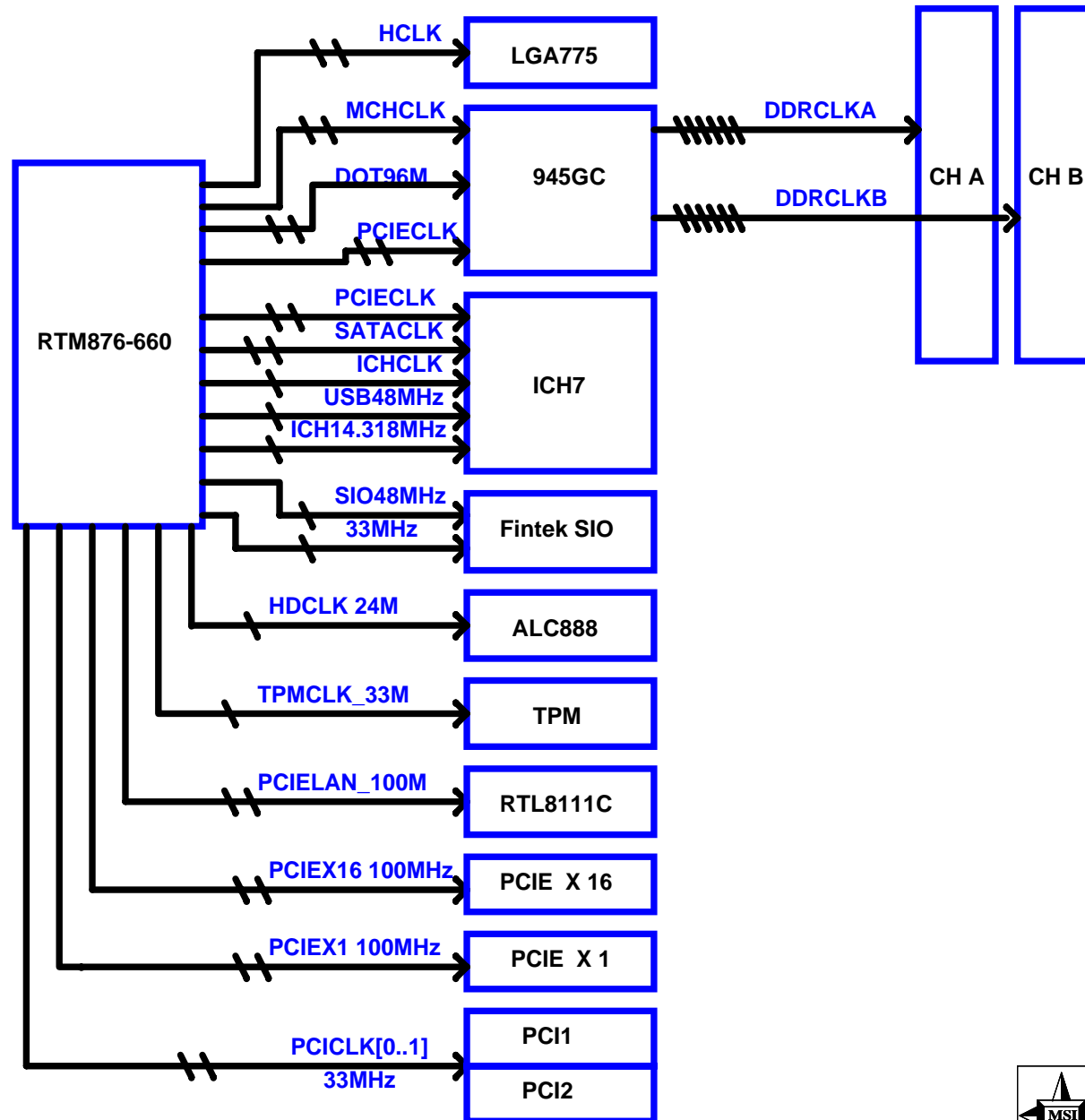
ST PWM:

Controller: 3 PHASES

Block Diagram



CLOCK MAP



MICRO-STAR INT'L CO.,LTD

MS-7313

Size Custom	Document Description CLOCK MAP	Rev 1.0
Date: Monday, December 10, 2007		
Sheet 3 of 33		

Processor
0.8375-1.6000V Core-125A
1.2V FSB Vtt-5.3A
VCCPLL
VCC-IOPLL & VCCA

945G/P MCH
1.2V FSB Vtt-0.9A
1.8V DDR2 I/O-4.4A(S0,S1)
1.8V DDR2 I/O-25mA(S3)
0.9V DDR2 VREF-2mA
0.9V DDR2 SB_VREF-10uA
DDR2 Resister Comp V-36mA
DDR2 Resis Comp SB_V-10uA
1.5V Core-13.8A(Integrated)
1.5V Core-8.9A(Discrete)
1.5V PCI Express&DMI-1.5A
1.5V PCIE&DMI PLL-45mA
1.5V HOST PLL-45mA
1.5V VCCA_DPLLA&B-55mA
1.5V MPLL-66mA
2.5V DAC-70mA*
2.5V HV-3mA
2.5V CMOS-2.0mA

ICH7
1.2V VCC_CPU-14mA
1.05V Core-0.86A
VCC1_5A*-1.01A
VCC1_5B*-0.77A
5VRef-6mA
5VrefSus-10mA
+3.3V-0.33A
RTC-6uA(G3)
3.3V VccSus*-52mA
VccSus1_05V-See Note 1
VccUSBPLL-10mA
VccDMIPLL-50mA
VccSATAIPLL-50mA

Battery

L6703 Regulator
VCCP
0.8375-1.6000V

VTT Regulator
V_FSB_VTT
1.2V

uP6103 Regulator
VCC_DDR
1.8V

uP6103 Regulator
V_1P5_CORE
1.5V

uP7707 Regulator
V_2P5_MCH
2.5V

1.05V Regulator
V_1P05_CORE
1.05V

uP7706 Regulator
3VSB
3.3V

uP7501 Regulator
5VDIMM
5V

W83310DS Regula
VTT_DDR
0.9V

DDR2 DIMM conn(4) & term
0.9V SM Vtt-1.2A(S0)
1.8V Vdd/vddq-4.7A(S0,S1)

PCIE X16 slot(1)
+12V-5.5A
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-3.0A

PCIE X1 slot(1)
+12V-0.5A
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-3.0A

PCI slot slot(4)
+3.3Vaux-375mA(wake)
+3.3Vaux-20mA(no wake)
+3.3V-7.6A
+5.0V-5.0A
+12V-0.5A
-12V-0.1A

USB
+5V-4A(S0,S1)

PS2
+5V-345mA(S0,S1)

CLKGEN
+3.3V-560mA

LAN
3VSB-

SIO
+3.3V
3VSB-

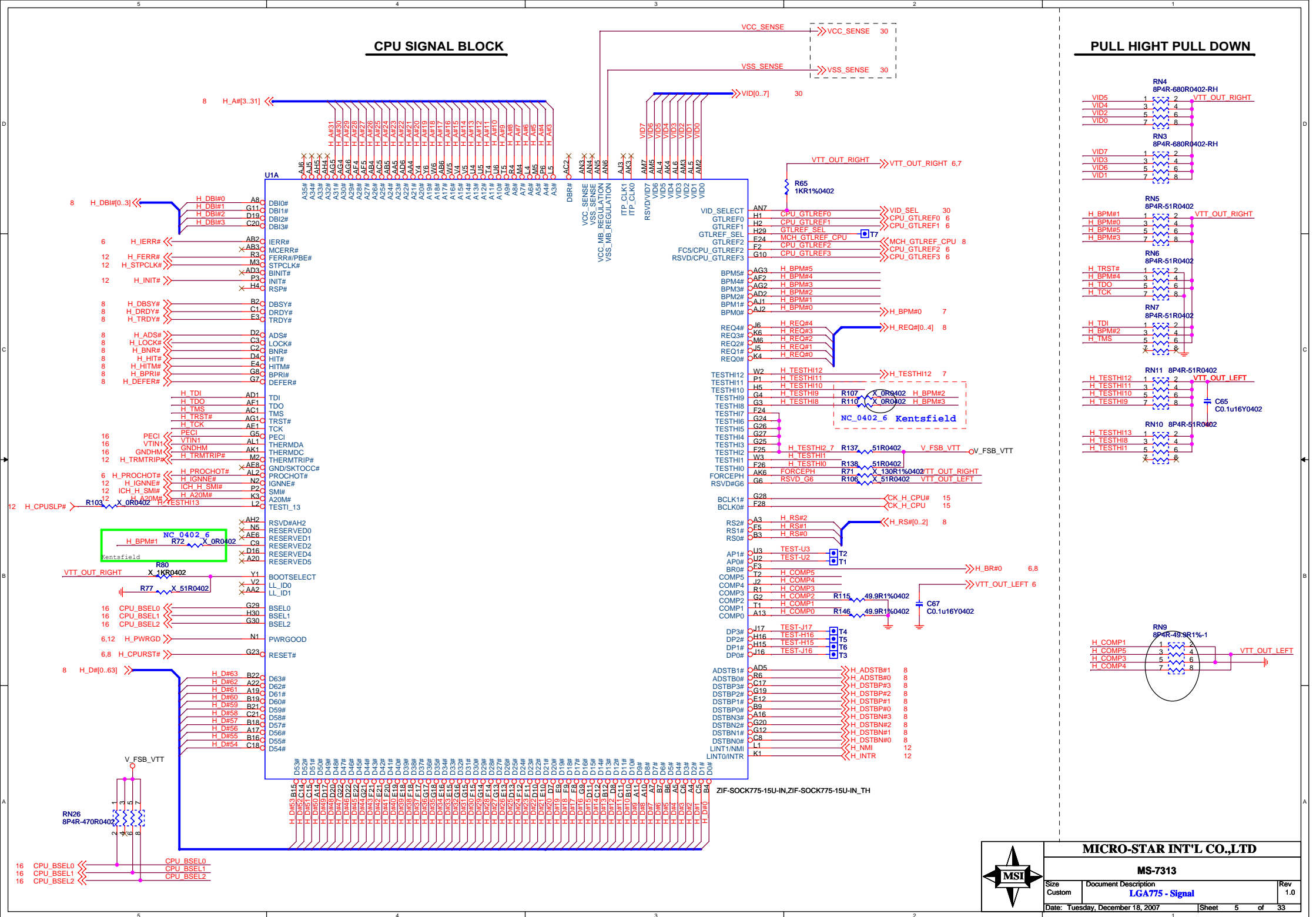
SPI ROM

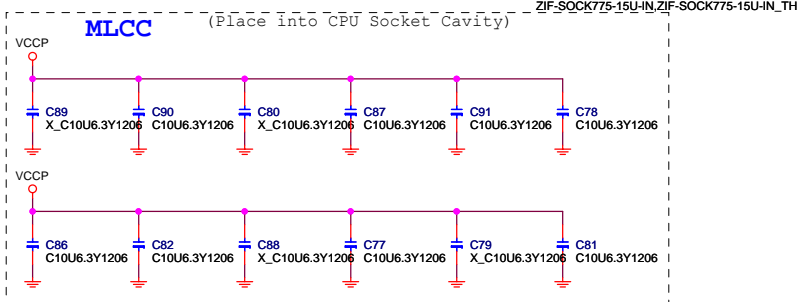
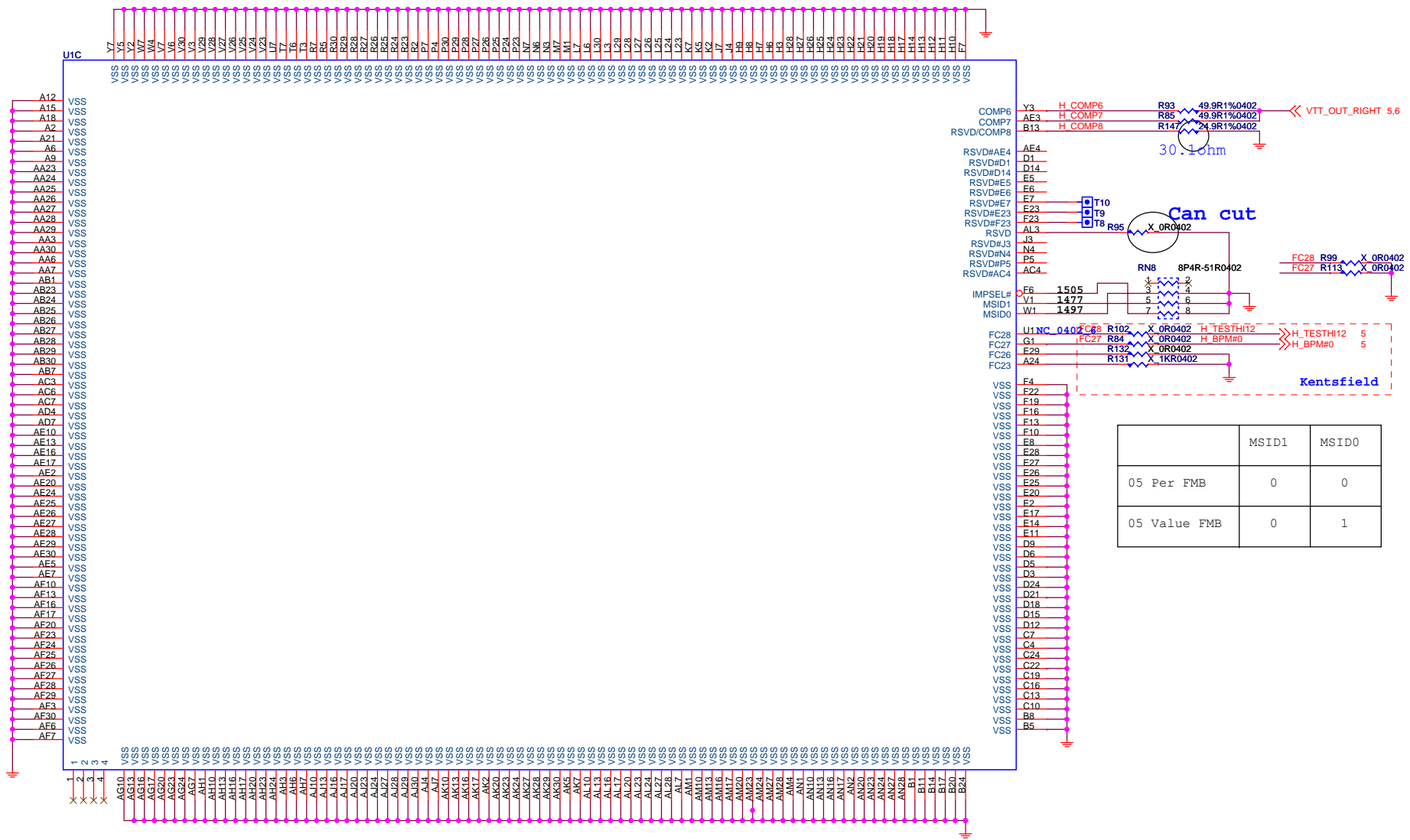
Audio Codec

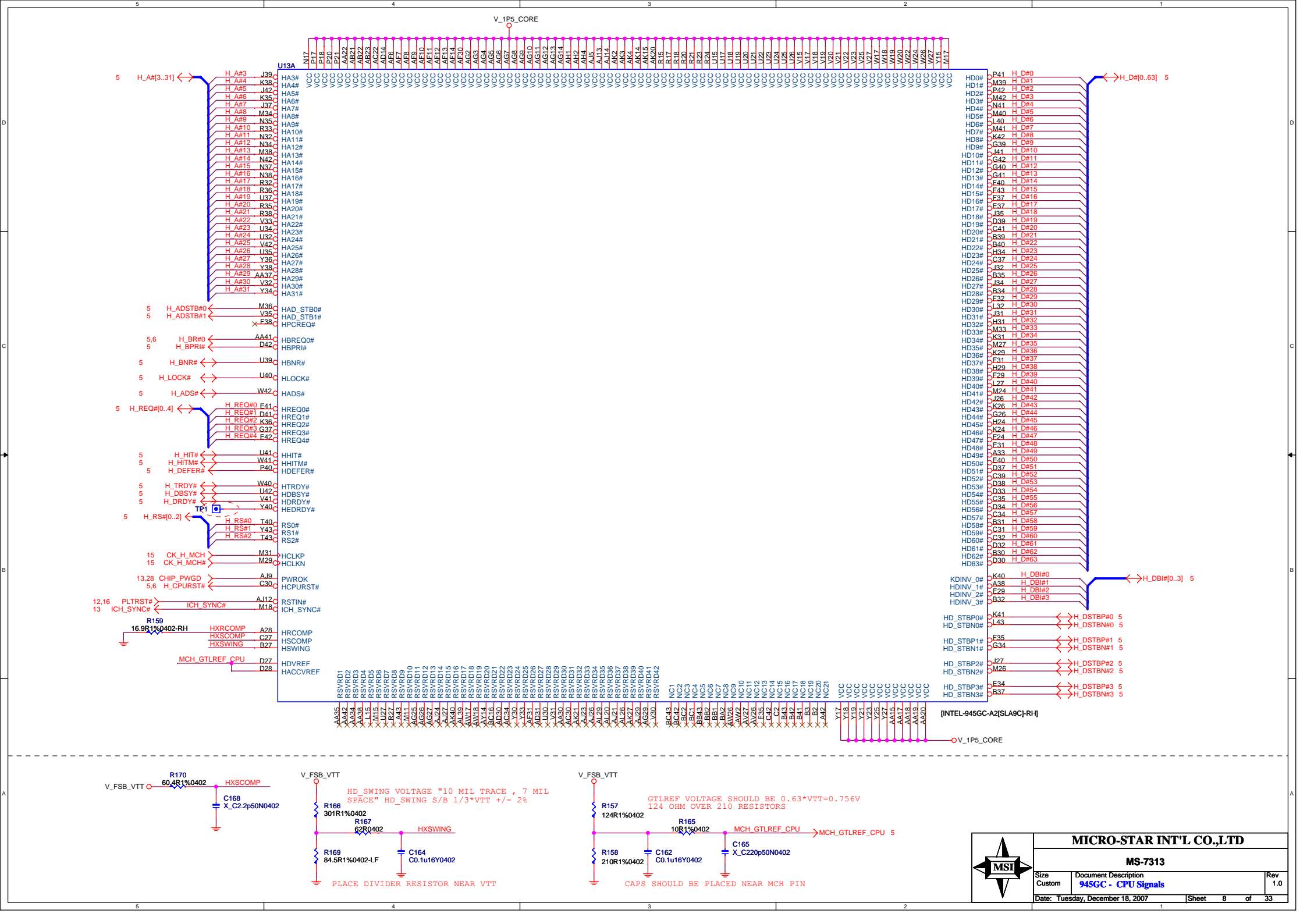
1394

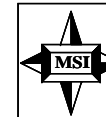
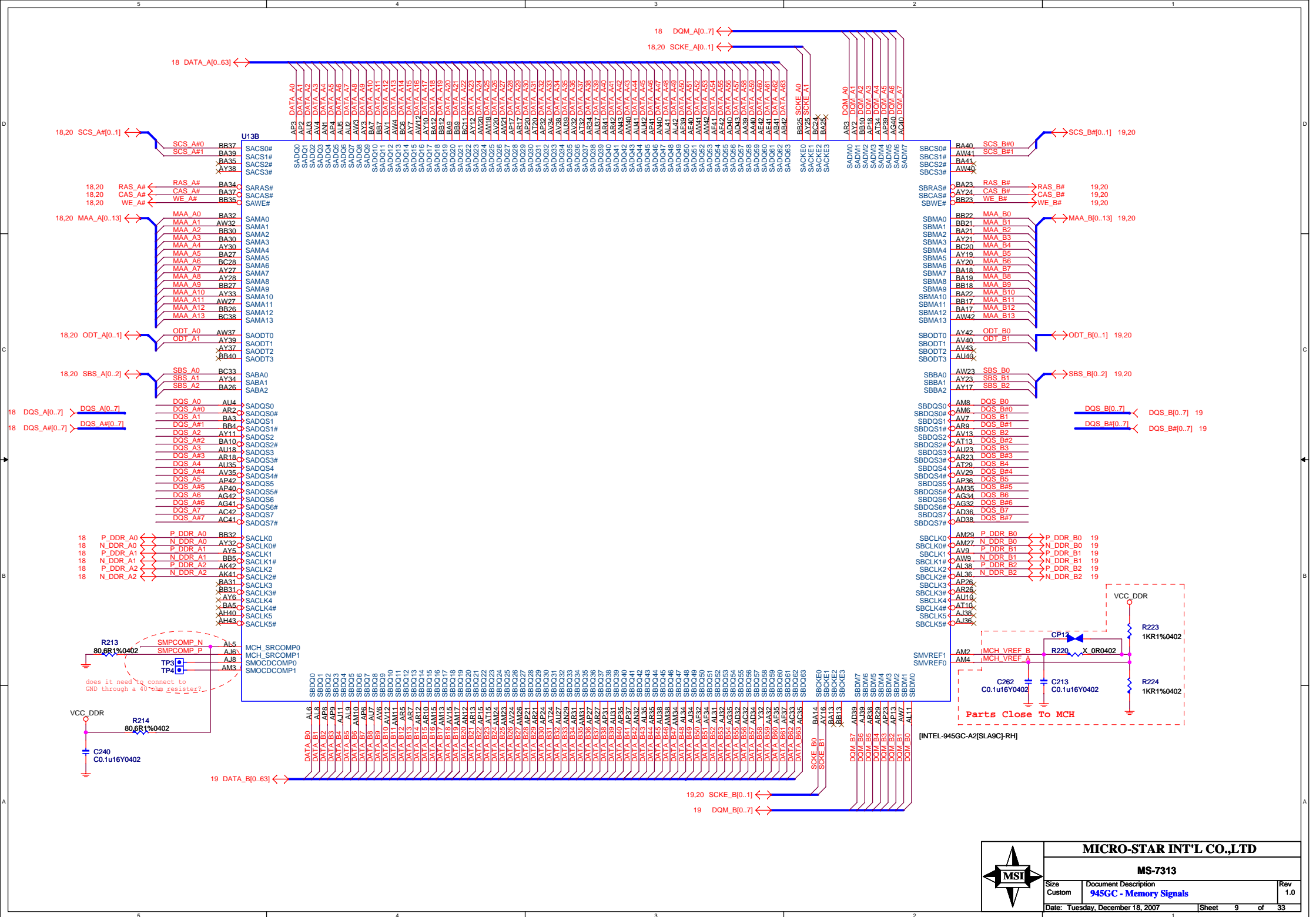
+12V
ATX 2x2

+12V	+5V	+3.3V	+5VSB
ATX POWER			





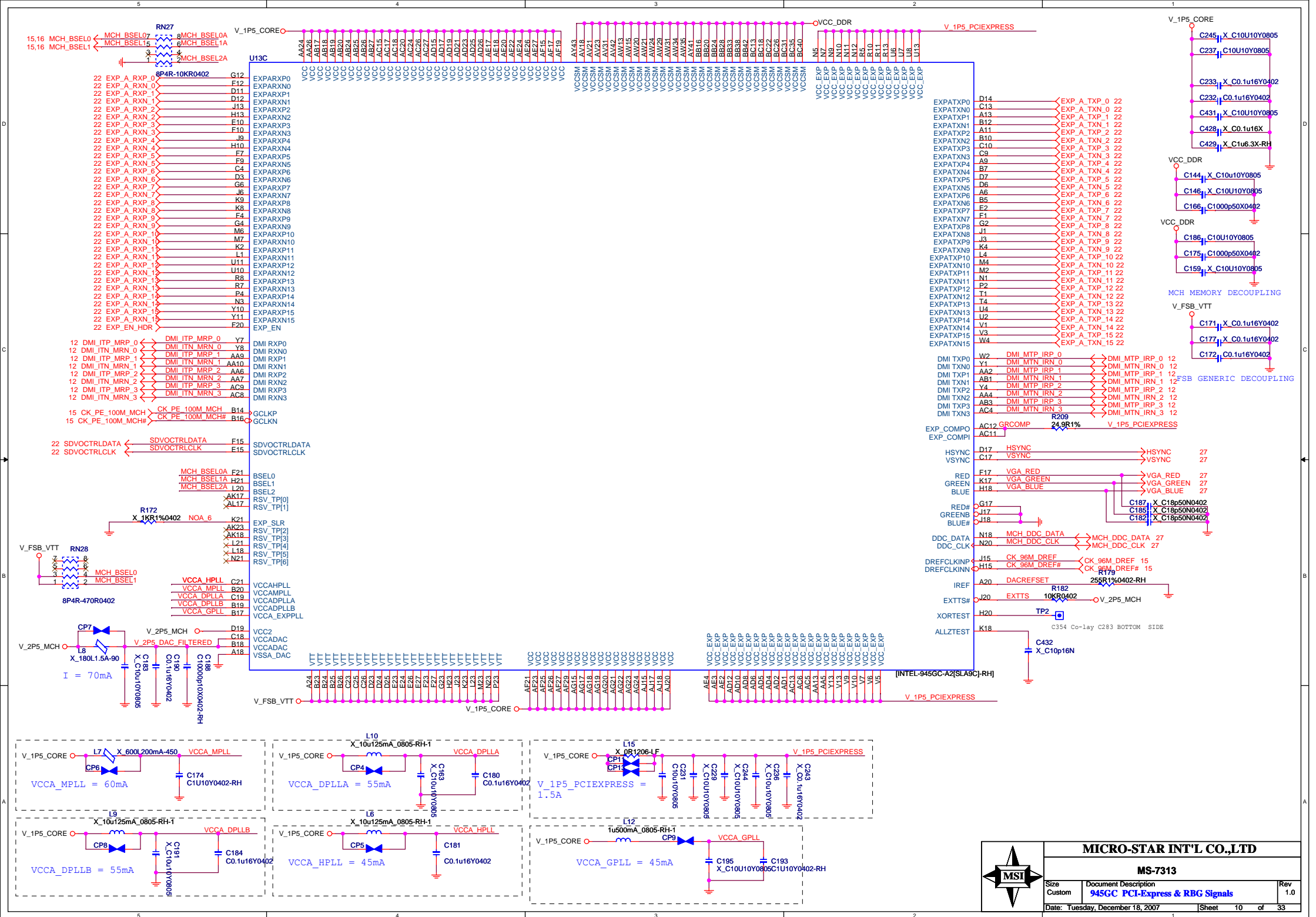




MICRO-STAR INT'L CO.,LTD

MS-7313

Size Custom	Document Description 945GC - Memory Signals	Rev 1.0
Date: Tuesday, December 18, 2007		Sheet 9 of 33

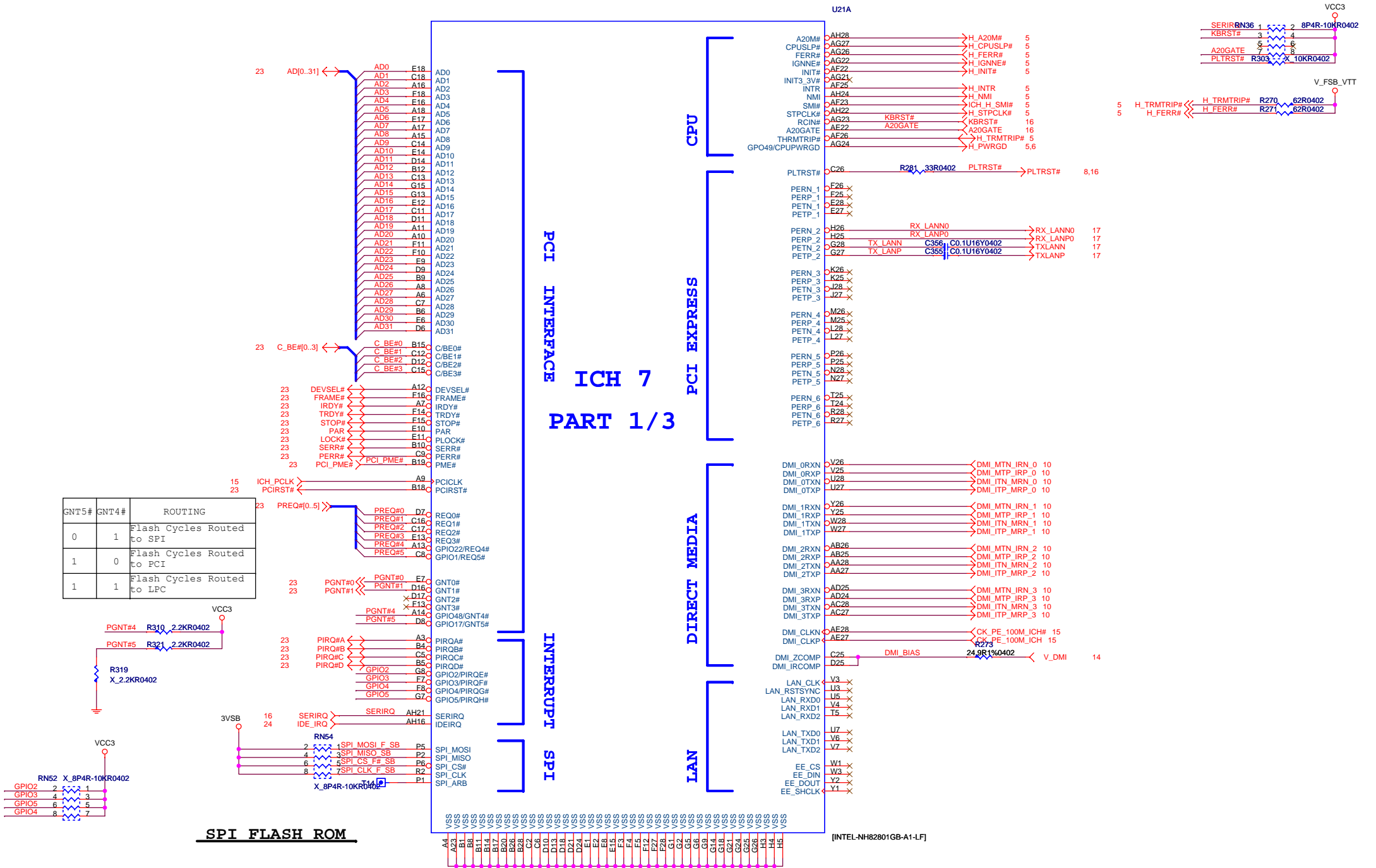




MICRO-STAR INT'L CO.,LTD

MS-7313

Size	Document Description	Rev
Custom	Intel 945GC - GND	1.0
Date: Tuesday, December 18, 2007		Sheet 11 of 33

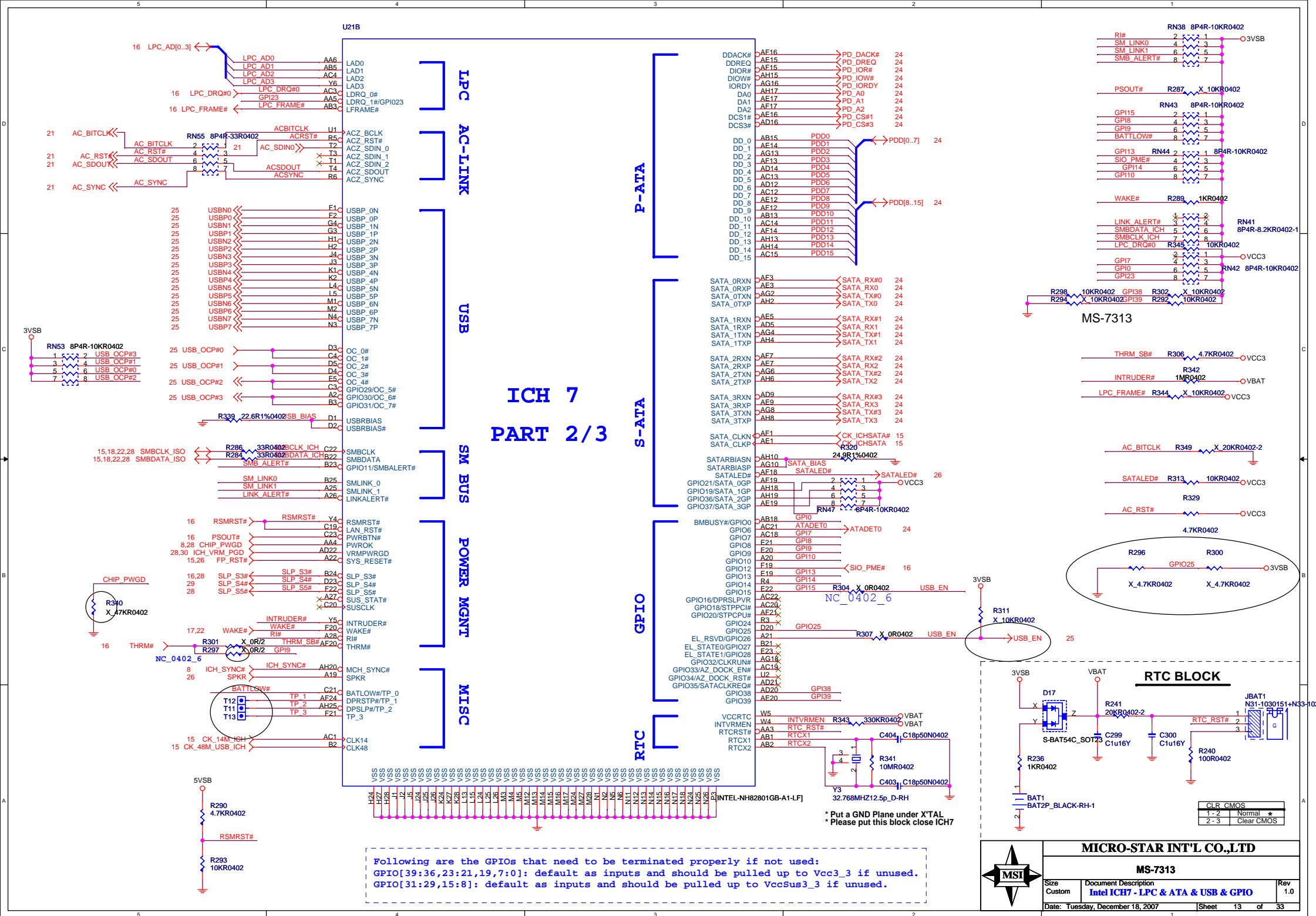


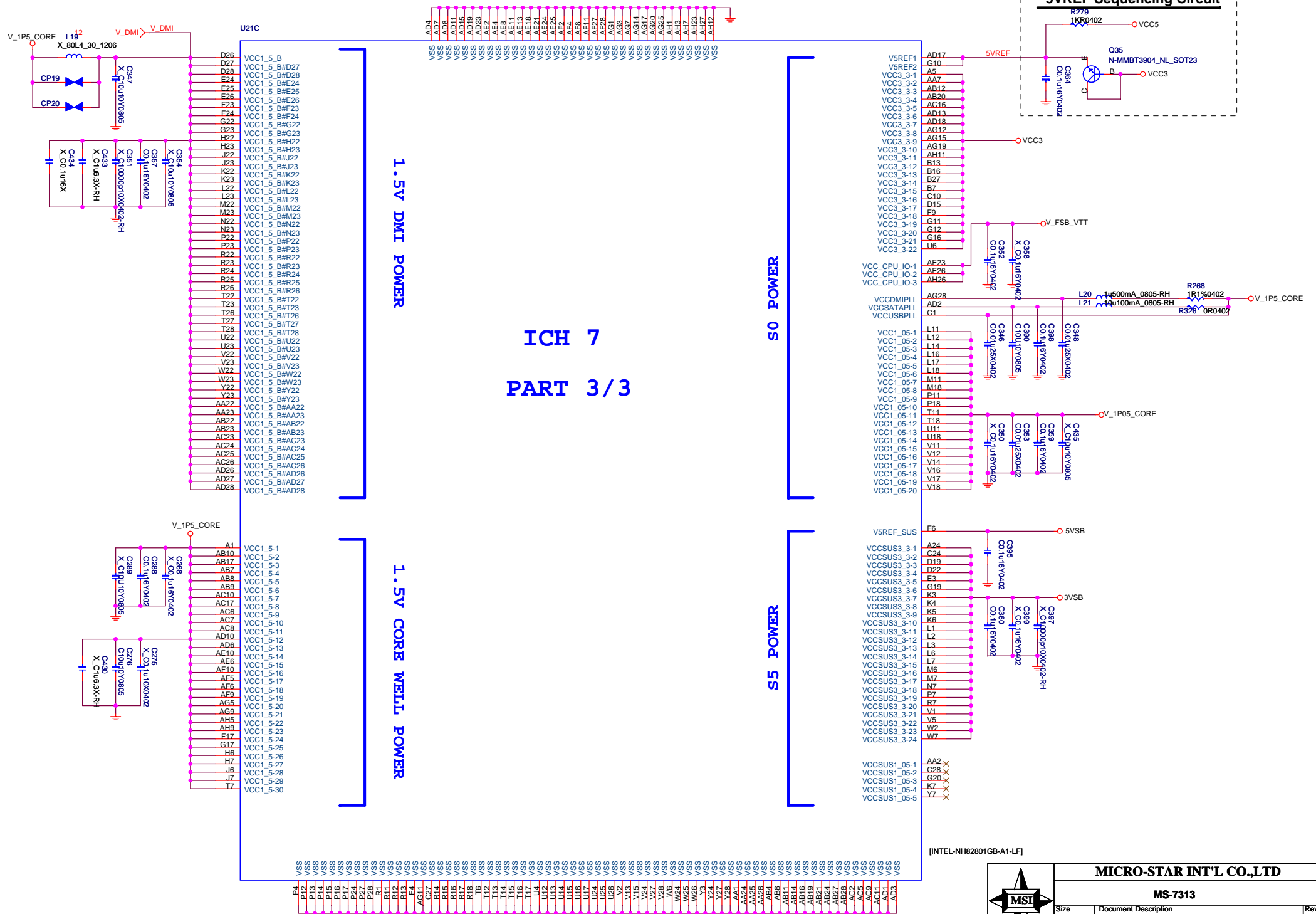
GNT5#	GNT4#	ROUTING
0	1	Flash Cycles Routed to SPI
1	0	Flash Cycles Routed to PCI
1	1	Flash Cycles Routed to LPC



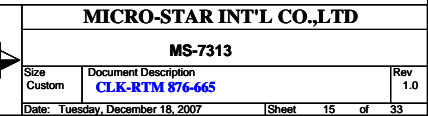
SPI FLASH ROM

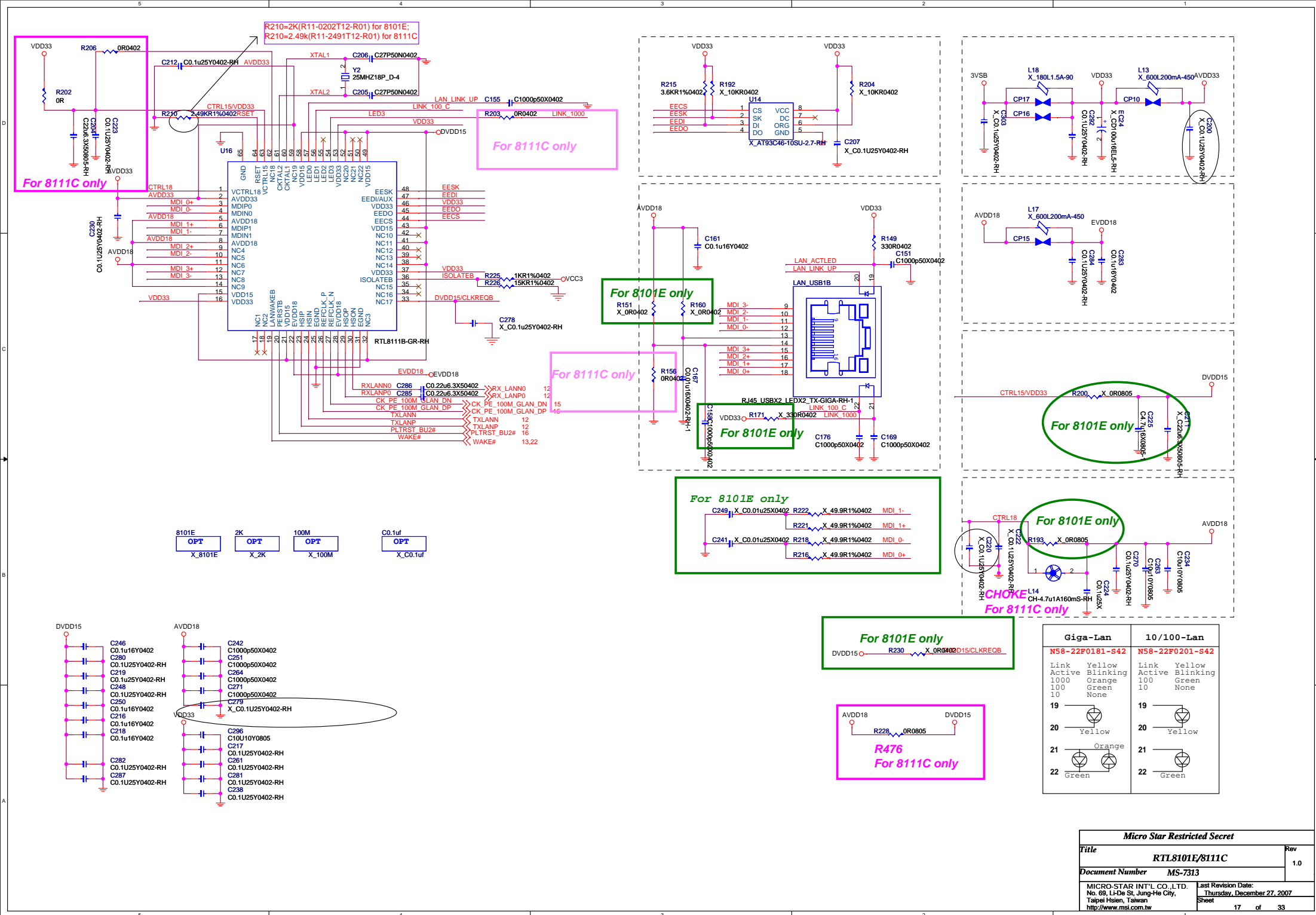






CPU Frequency Selection			
FS_C	FS_B	FS_A	CPU
0	0	1	133M
0	1	0	200M
0	0	0	266M
1	0	0	333M
1	1	0	400M





9,20 MAA_A[0..13] <- MAA_A[0..13]
9 DATA_A[0..63] <- DATA_A[0..63]
9 DQM_A[0..7] <- DQM_A[0..7]

DDR2 DIMM A

DIMM1

DATA A0 3
DATA A1 4
DATA A2 9
DATA A3 10
DATA A4 122
DATA A5 123
DATA A6 128
DATA A7 129
DATA A8 12
DATA A9 13
DATA A10 21
DATA A11 22
DATA A12 131
DATA A13 132
DATA A14 140
DATA A15 141
DATA A16 24
DATA A17 25
DATA A18 30
DATA A19 31
DATA A20 143
DATA A21 144
DATA A22 149
DATA A23 150
DATA A24 33
DATA A25 34
DATA A26 39
DATA A27 40
DATA A28 152
DATA A29 153
DATA A30 158
DATA A31 159
DATA A32 80
DATA A33 81
DATA A34 86
DATA A35 87
DATA A36 199
DATA A37 200
DATA A38 205
DATA A39 206
DATA A40 89
DATA A41 90
DATA A42 95
DATA A43 96
DATA A44 208
DATA A45 209
DATA A46 214
DATA A47 215
DATA A48 98
DATA A49 99
DATA A50 107
DATA A51 108
DATA A52 217
DATA A53 218
DATA A54 226
DATA A55 227
DATA A56 110
DATA A57 111
DATA A58 116
DATA A59 117
DATA A60 229
DATA A61 230
DATA A62 235
DATA A63 236

2 VSS
5 VSS
8 VSS
11 VSS
14 VSS
17 VSS
20 VSS
23 VSS
26 VSS
29 VSS
32 VSS
35 VSS
38 VSS
41 VSS
44 VSS
47 VSS
50 VSS
53 VSS
56 VSS
59 VSS
62 VSS
65 VSS
68 VSS
71 VSS
74 VSS
77 VSS
80 VSS
83 VSS
86 VSS
89 VSS
92 VSS
95 VSS
98 VSS
101 VSS
104 VSS
107 VSS
110 VSS
113 VSS
116 VSS
119 VSS
122 VSS
125 VSS
128 VSS
131 VSS
134 VSS
137 VSS
140 VSS
143 VSS
146 VSS
149 VSS
152 VSS
155 VSS
158 VSS
161 VSS
164 VSS
167 VSS
170 VSS
173 VSS
176 VSS
179 VSS
182 VSS
185 VSS
188 VSS
191 VSS
194 VSS
197 VSS
200 VSS
203 VSS
206 VSS
209 VSS
212 VSS
215 VSS
218 VSS
221 VSS
224 VSS
227 VSS
230 VSS
233 VSS
236 VSS

100
103
106
109
112
115
118
121
124
127
130
133
136
139
142
145
148
151
154
157
160
163
166
169
172
175
178
181
184
187
190
193
196
199
202
205
208
211
214
217
220
223
226
229
232
235
238
241
244
247
250
253
256
259
262
265
268
271
274
277
280
283
286
289
292
295
298
301
304
307
310
313
316
319
322
325
328
331
334
337
340
343
346
349
352
355
358
361
364
367
370
373
376
379
382
385
388
391
394
397

DDRII-240_GREEN-RH

9 DQS_A[0..7] <- DQS_A[0..7]
9 DQS_A#[0..7] <- DQS_A#[0..7]

DQ0
DQ1
DQ2
DQ3
DQ4
DQ5
DQ6
DQ7
DQ8
DQ9
DQ10
DQ11
DQ12
DQ13
DQ14
DQ15
DQ16
DQ17
DQ18
DQ19
DQ20
DQ21
DQ22
DQ23
DQ24
DQ25
DQ26
DQ27
DQ28
DQ29
DQ30
DQ31
DQ32
DQ33
DQ34
DQ35
DQ36
DQ37
DQ38
DQ39
DQ40
DQ41
DQ42
DQ43
DQ44
DQ45
DQ46
DQ47
DQ48
DQ49
DQ50
DQ51
DQ52
DQ53
DQ54
DQ55
DQ56
DQ57
DQ58
DQ59
DQ60
DQ61
DQ62
DQ63

125 DQM A0
126 DQM A1
127 DQM A2
128 DQM A3
129 DQM A4
130 DQM A5
131 DQM A6
132 DQM A7
133 DQM A8
134 DQM A9
135 DQM A10
136 DQM A11
137 DQM A12
138 DQM A13
139 DQM A14
140 DQM A15
141 DQM A16
142 DQM A17
143 DQM A18
144 DQM A19
145 DQM A20
146 DQM A21
147 DQM A22
148 DQM A23
149 DQM A24
150 DQM A25
151 DQM A26
152 DQM A27
153 DQM A28
154 DQM A29
155 DQM A30
156 DQM A31
157 DQM A32
158 DQM A33
159 DQM A34
160 DQM A35
161 DQM A36
162 DQM A37
163 DQM A38
164 DQM A39
165 DQM A40
166 DQM A41
167 DQM A42
168 DQM A43
169 DQM A44
170 DQM A45
171 DQM A46
172 DQM A47
173 DQM A48
174 DQM A49
175 DQM A50
176 DQM A51
177 DQM A52
178 DQM A53
179 DQM A54
180 DQM A55
181 DQM A56
182 DQM A57
183 DQM A58
184 DQM A59
185 DQM A60
186 DQM A61
187 DQM A62
188 DQM A63

SPD Add. = A0

193 SCS_A#0 <- SCS_A#0 9,20
194 SCS_A#1 <- SCS_A#1 9,20

195 ODT A0 <- ODT A0 9,20
196 ODT A1 <- ODT A1 9,20

197 SCKE A0 <- SCKE A0 9,20
198 SCKE A1 <- SCKE A1 9,20

199 P_DDR A0 <- P_DDR A0 9
200 N_DDR A0 <- N_DDR A0 9

201 P_DDR A1 <- P_DDR A1 9
202 N_DDR A1 <- N_DDR A1 9

203 P_DDR A2 <- P_DDR A2 9
204 N_DDR A2 <- N_DDR A2 9

205 SMBCLK_DDR <- SMBCLK_DDR 19
206 SMBDATA_DDR <- SMBDATA_DDR 19

207 DIMM VREF A
208 VREF A

209 SA0
210 SA1
211 SA2

212 C210
213 C0.1u16Y0402
214 PLACE CLOSE
215 TO DIMM PIN

216 R211
217 1KR1%0402
218 R212
219 1KR1%0402

220

221

222

223

224

225

226

227

228

229

230

231

232

233

234

235

236

237

238

239

240

241

242

243

244

245

246

247

248

249

250

251

252

253

254

255

256

257

258

259

260

261

262

263

264

265

266

267

268

269

270

271

272

273

274

275

276

277

278

279

280

281

282

283

284

285

286

287

288

289

290

291

292

293

294

295

296

297

298

299

300

301

302

303

304

305

306

307

308

309

310

311

312

313

314

315

316

317

318

319

320

321

322

323

324

325

326

327

328

329

330

331

332

333

334

335

336

337

338

339

340

341

342

343

344

345

346

347

348

349

350

351

352

353

354

355

356

357

358

359

360

361

362

363

364

365

366

367

368

369

370

371

372

373

374

375

376

377

378

379

380

381

382

383

384

385

386

387

388

389

390

391

392

393

394

395

396

397

398

399

400

401

402

403

404

405

406

407

408

409

410

411

412

413

414

415

416

417

418

419

420

421

422

423

424

425

426

427

428

429

430

431

432

433

434

435

436

437

438

439

440

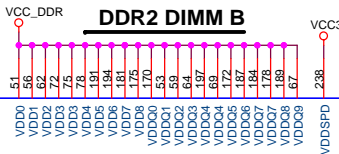
441

442

443

<

9,20 MAA_B[0..13] <-> MAA_B[0..13]
9 DATA_B[0..63] <-> DATA_B[0..63]
9 DQM_B[0..7] <-> DQM_B[0..7]



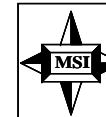
9 DQS_B[0..7] <-> DQS_B[0..7]
9 DQS_B#[0..7] <-> DQS_B#[0..7]

DATA_B0 3
DATA_B1 4
DATA_B2 9
DATA_B3 10
DATA_B4 122
DATA_B5 123
DATA_B6 128
DATA_B7 129
DATA_B8 12
DATA_B9 13
DATA_B10 21
DATA_B11 22
DATA_B12 131
DATA_B13 132
DATA_B14 140
DATA_B15 141
DATA_B16 24
DATA_B17 25
DATA_B18 30
DATA_B19 31
DATA_B20 143
DATA_B21 144
DATA_B22 149
DATA_B23 150
DATA_B24 33
DATA_B25 34
DATA_B26 39
DATA_B27 40
DATA_B28 152
DATA_B29 153
DATA_B30 158
DATA_B31 159
DATA_B32 80
DATA_B33 81
DATA_B34 86
DATA_B35 87
DATA_B36 199
DATA_B37 200
DATA_B38 205
DATA_B39 206
DATA_B40 89
DATA_B41 90
DATA_B42 95
DATA_B43 96
DATA_B44 208
DATA_B45 209
DATA_B46 214
DATA_B47 215
DATA_B48 98
DATA_B49 99
DATA_B50 107
DATA_B51 108
DATA_B52 217
DATA_B53 218
DATA_B54 226
DATA_B55 227
DATA_B56 110
DATA_B57 111
DATA_B58 116
DATA_B59 117
DATA_B60 229
DATA_B61 230
DATA_B62 235
DATA_B63 236

DO0
DO1
DO2
DO3
DO4
DO5
DO6
DO7
DO8
DO9
DO10
DO11
DO12
DO13
DO14
DO15
DO16
DO17
DO18
DO19
DO20
DO21
DO22
DO23
DO24
DO25
DO26
DO27
DO28
DO29
DO30
DO31
DO32
DO33
DO34
DO35
DO36
DO37
DO38
DO39
DO40
DO41
DO42
DO43
DO44
DO45
DO46
DO47
DO48
DO49
DO50
DO51
DO52
DO53
DO54
DO55
DO56
DO57
DO58
DO59
DO60
DO61
DO62
DO63

ODT0
ODT1
CKE0
CKE1
CS0#
CS1#
CK0(DU)
CK0#(DU)
CK1(CK0)
CK1#(CK0#)
CK2(DU)
CK2#(DU)
SCL
SDA
X1
X2
VREF
SA0
SA1
SA2
SPD Add. = A4

DDR11-240_ORANGE-RH

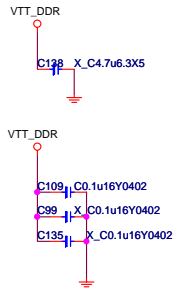


MICRO-STAR INT'L CO.,LTD

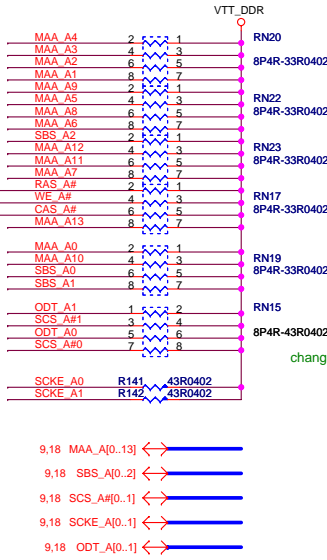
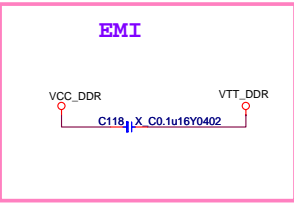
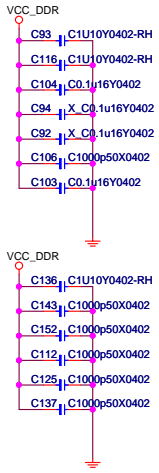
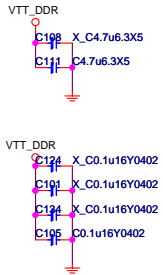
MS-7313

Size	Document Description	Rev
Custom	DDR II DIMM A & B	1.0
Date: Tuesday, December 18, 2007		Sheet 19 of 33

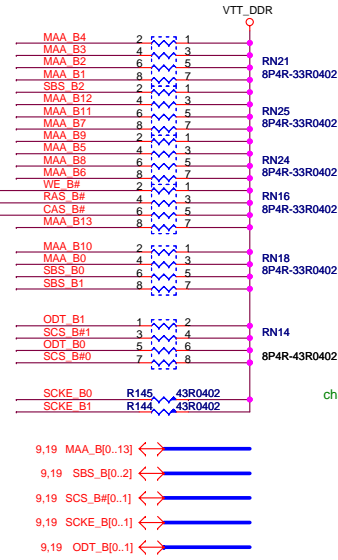
CHANNEL A V_SM_VTT DECOUPLING CAPS



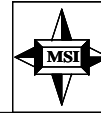
CHANNEL B V_SM_VTT DECOUPLING CAPS

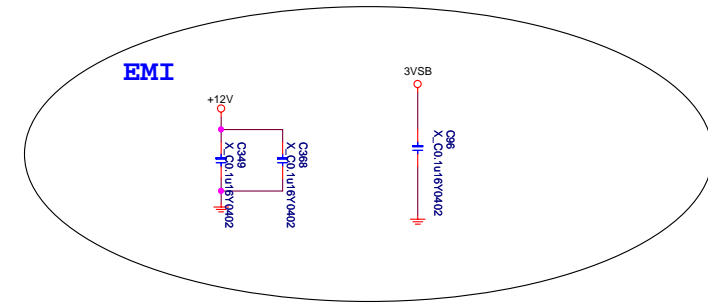
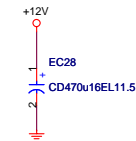
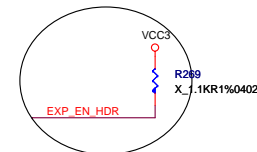


change RN



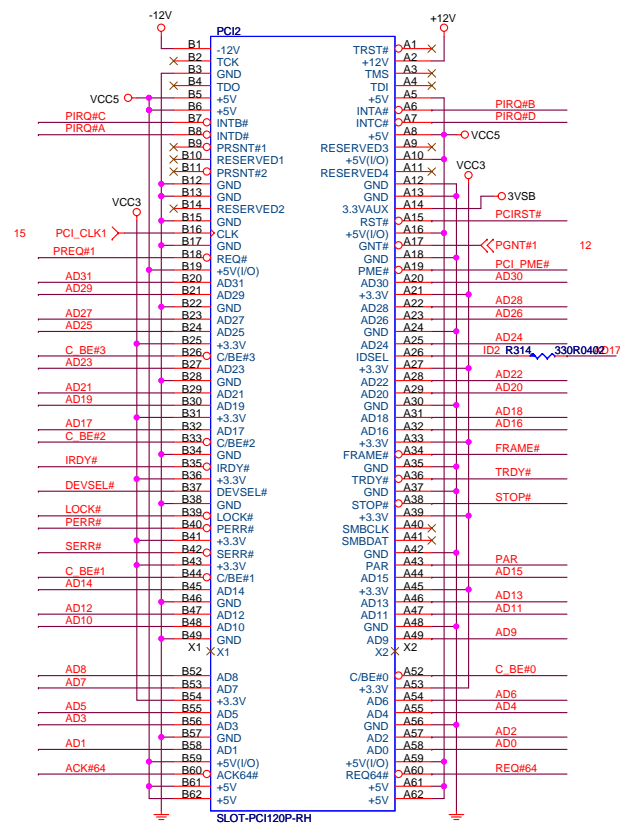
change RN





Size Custom	Document Description PCI EXPRESSX16&X1	Rev 1.0
Date: Tuesday, December 18, 2007	Sheet 22 of 33	

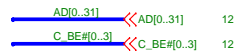
PCI SLOT 2 (PCI VER: 2.2 COMPLY)



```

IDSEL = AD17
MASTER = PREQ#1
PIRQ#B

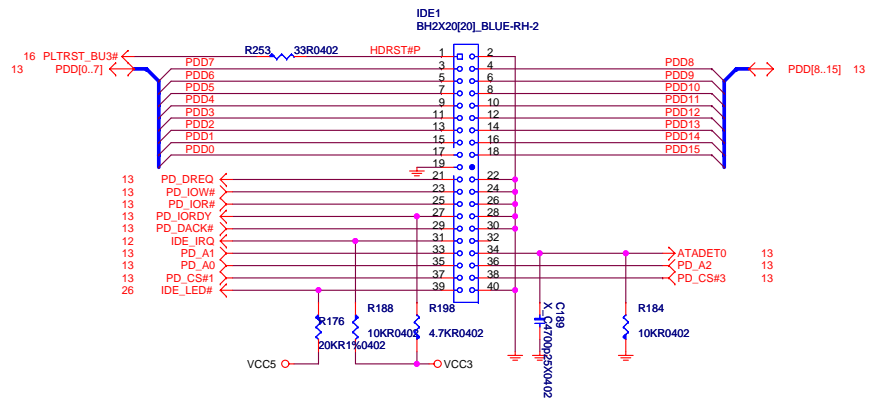
```



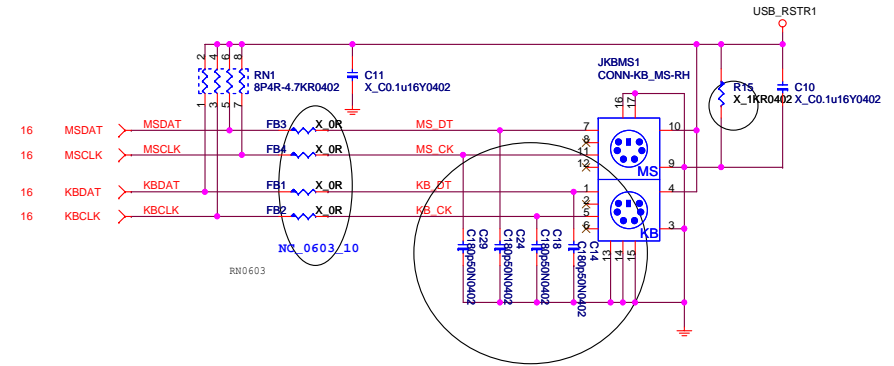
MS-7313

Size Custom	Document Description PCI Slot 1 &2	Rev 1.0
Date: Tuesday, December 18, 2007		Sheet 23 of 33

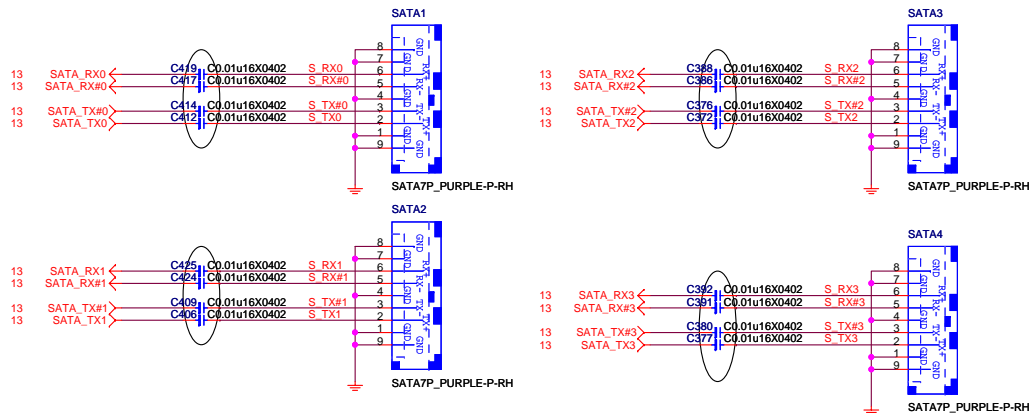
ATA 33/66/100 IDE Connectors



PS2 KEYBOARD & MOUSE CONNECTOR



SERIAL ATA CONNECTOR BLOCK

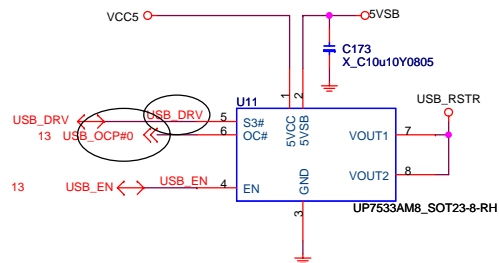


MICRO-STAR INT'L CO.,LTD

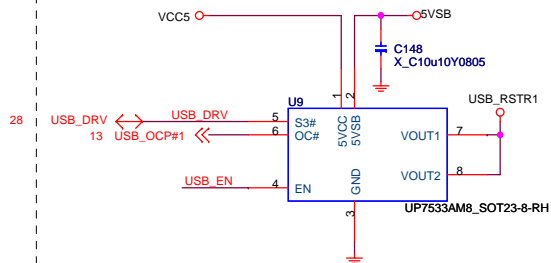
MS-7313

Size Custom	Document Description IDE & SATA Connectors	Rev 1.0
Date: Tuesday, December 18, 2007		Sheet 24 of 33

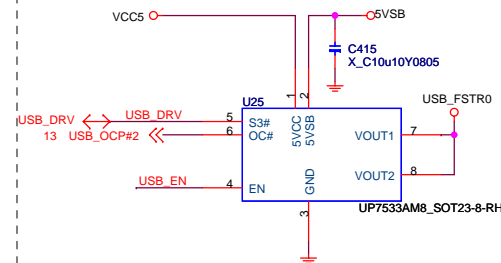
POWER CIRCUIT FOR USB PORT 0,1



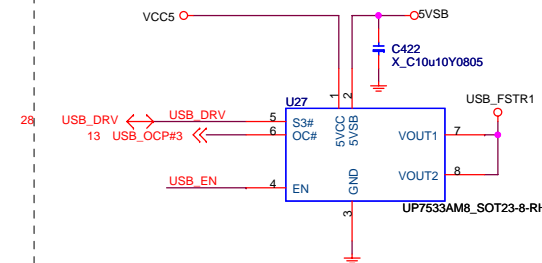
POWER CIRCUIT FOR USB PORT 2,3



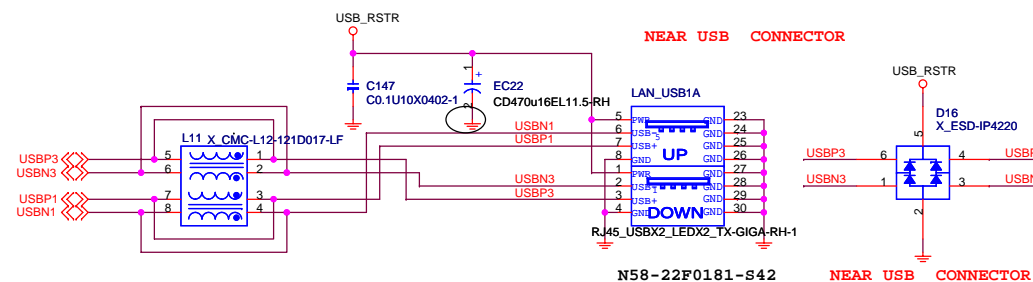
POWER CIRCUIT FOR USB PORT 4,5



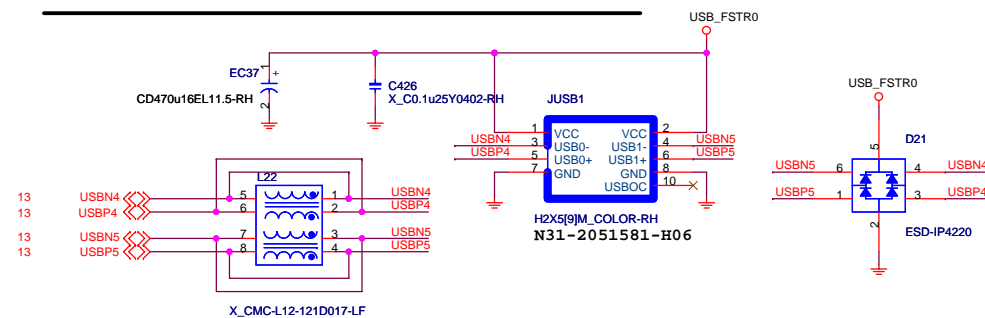
POWER CIRCUIT FOR USB PORT 6,7



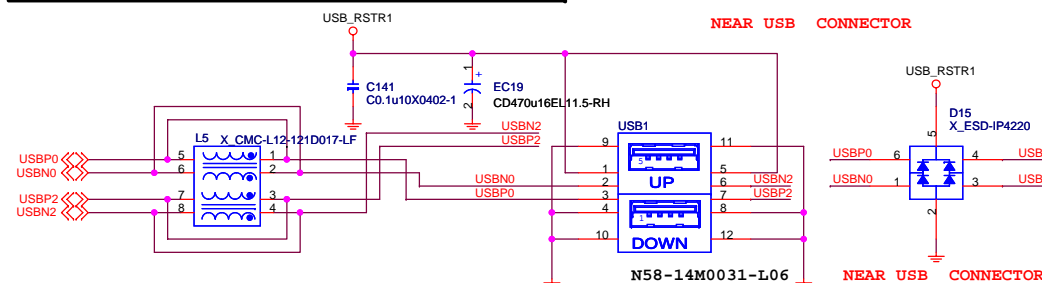
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



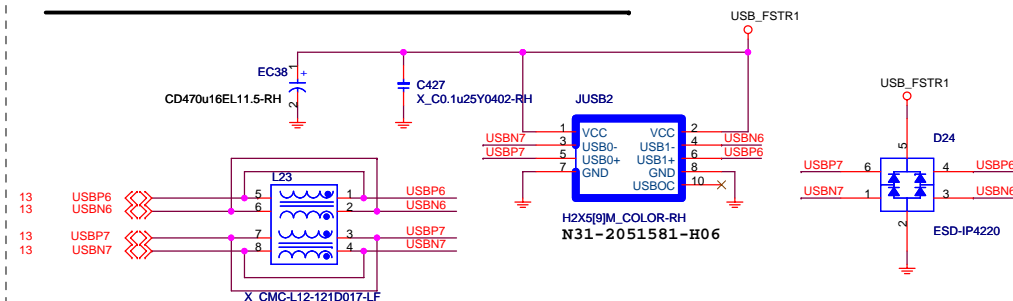
FRONT PANEL USB CONNECTOR FOR USB PORT 4,5



REAR PANEL USB CONNECTOR FOR USB PORT 2,3



FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



MICRO-STAR INT'L CO.,LTD

MS-7313

Size	Document Description	Rev
Custom	USB CONNECTORS	1.0
Date: Thursday, December 20, 2007	Sheet 25 of 33	

The diagram shows two LED drivers. The top driver uses a PNP transistor Q36 (N-MMBT3904_NL_SOT23) to drive the SUS_LED. Its emitter is connected to 5VSB, its base is connected to a resistor RN39 (8P4R-330R0402) which is in series with the LED's anode, and its collector is connected to the LED's cathode. The bottom driver uses an NPN transistor Q37 (N-MMBT3904_NL_SOT23) to drive the PWR_LED. Its emitter is connected to ground, its base is connected to a resistor RN46 (8P4R-4.7KR0402) which is in series with the LED's anode, and its collector is connected to the LED's cathode. The LEDs are labeled SUS_LED and PWR_LED in red. The input signals are LED_VCC and LED_VSB, also in red. A pink box highlights the bottom driver circuit.

SYSTEM FAN

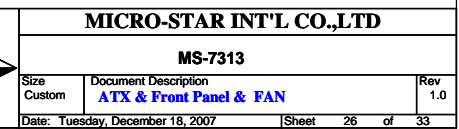
The schematic diagram illustrates the electrical connection for the system fan. A +12V supply is connected to a series combination of resistors R42 (4.7K R0402) and R48 (27K R0402). The output of this series combination is connected to the fan, SYSFAN2, and also to a resistor R53 (10K R0402) which is connected to ground. A capacitor C9 (X_C10u16x51206-RH) is connected in parallel with the fan. The fan is labeled H1X3B-FR_WHITE-RH. The output signal is labeled SYS_FAN1.

PWR FAN

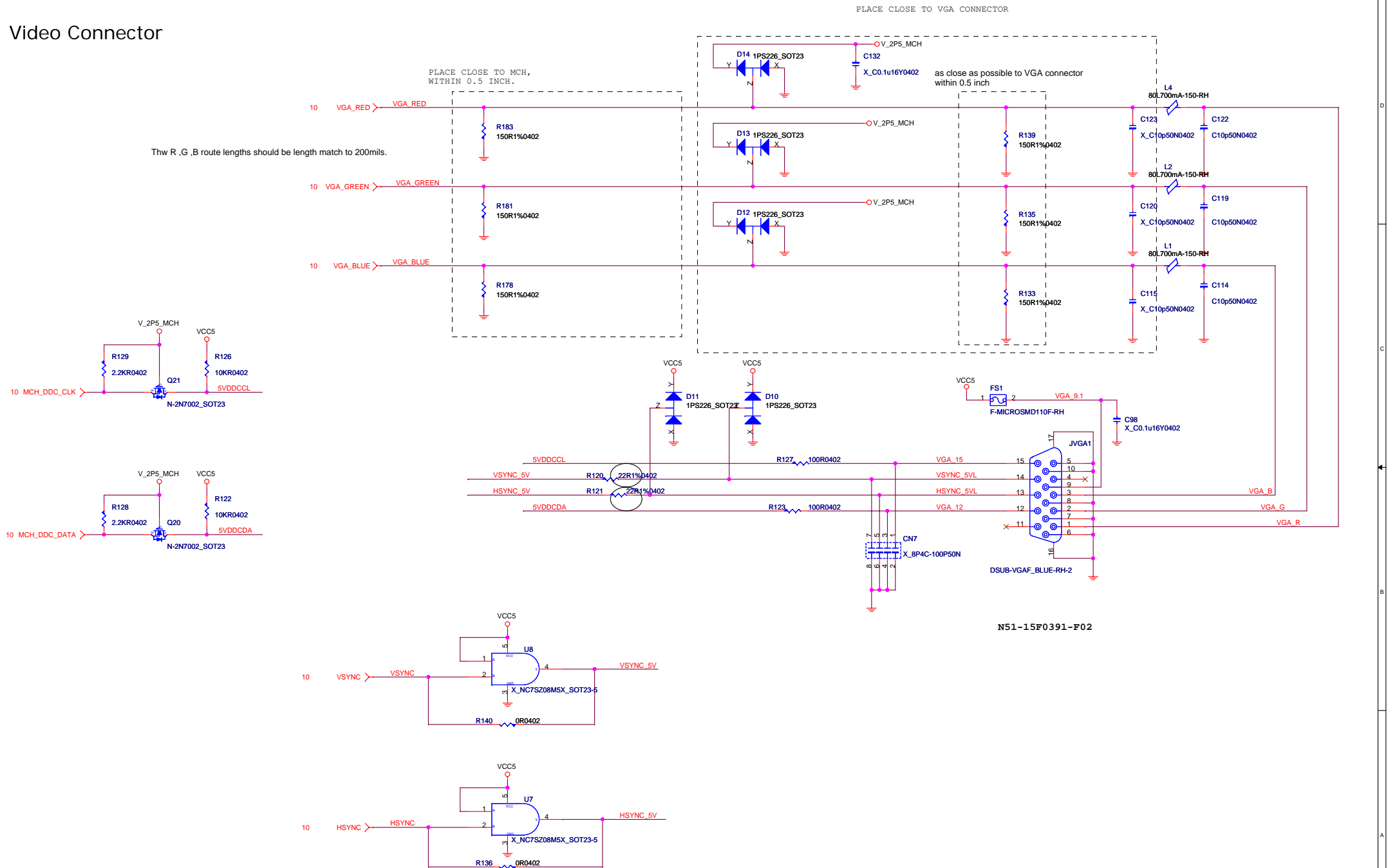
The schematic diagram illustrates the PWR FAN circuit. It features a +12V power supply connected to a network of resistors and a capacitor. The circuit includes a fan (SYSFAN1) and a signal output (SYS_FAN2).

Key components and connections:

- Power Supply:** +12V
- Resistors:**
 - R60: 4.7KΩ0402
 - R61: 27KΩ0402
 - R66: 10KΩ0402
- Capacitor:** C49: X_C10u16X51206-RH
- Fan:** SYSFAN1 (AH1X3B-FR_WHITE-RH)
- Signal Output:** SYS_FAN2 (16)



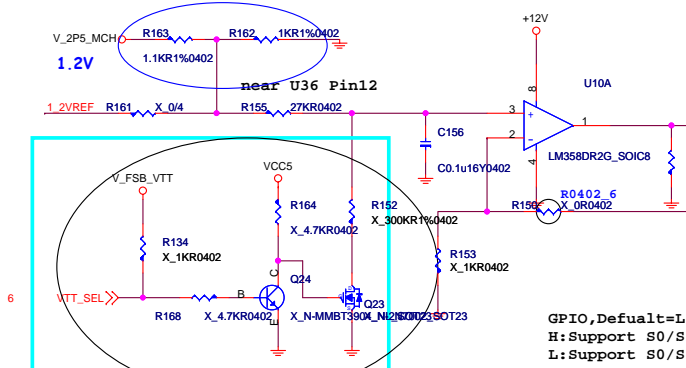
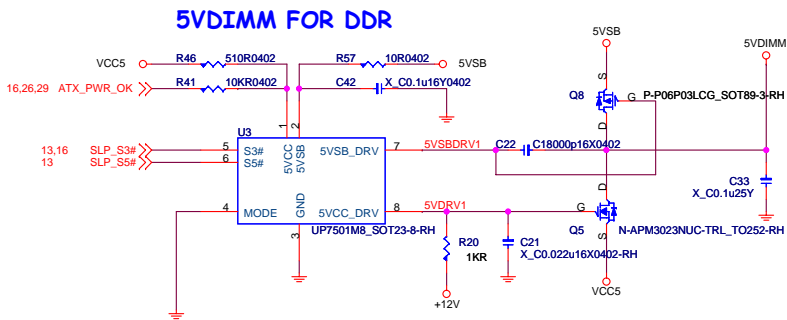
Video Connector



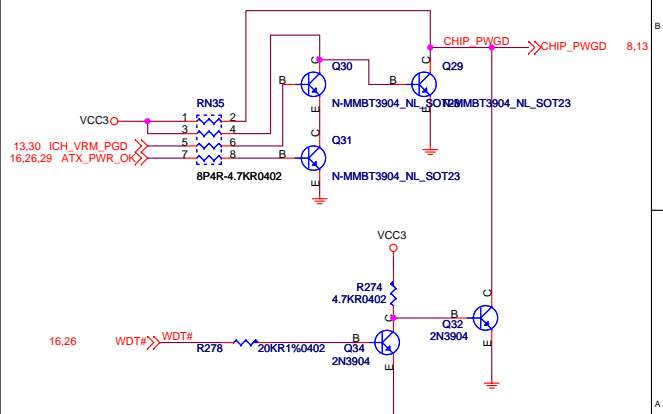
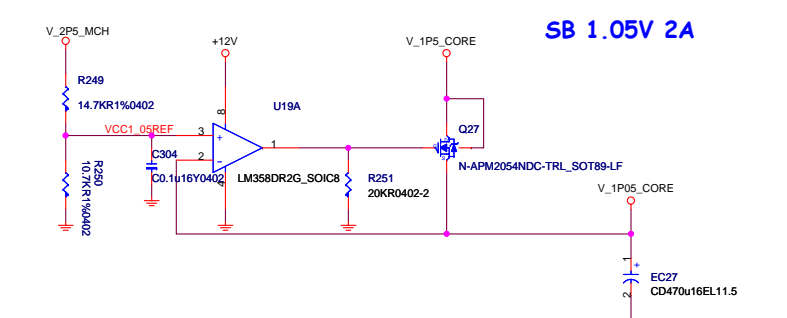
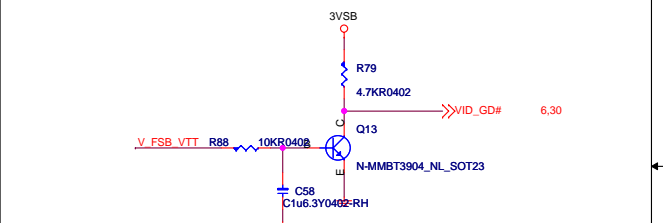
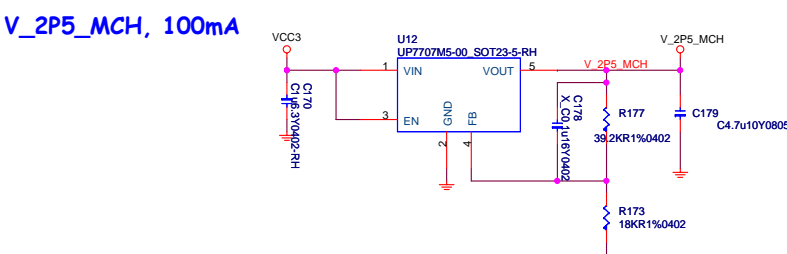
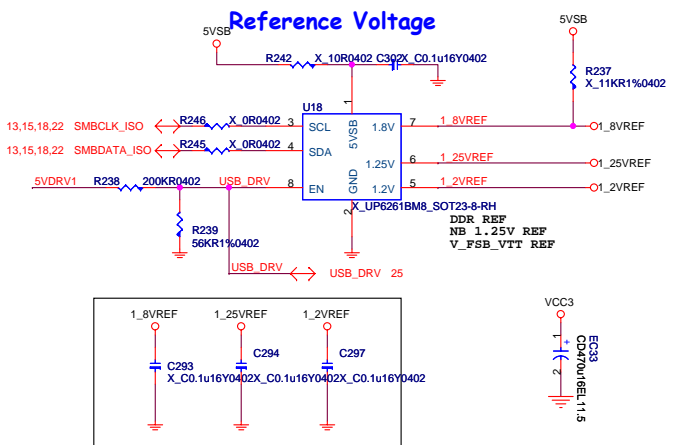
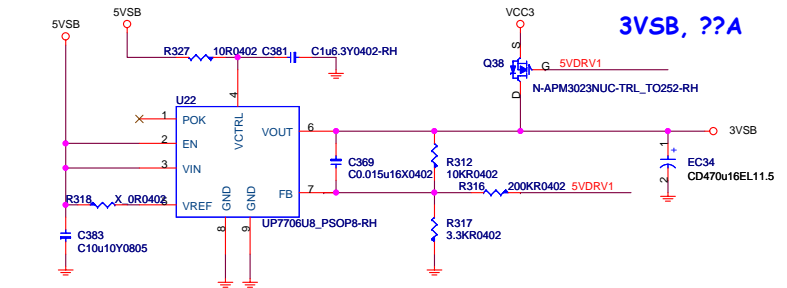
MICRO-STAR INT'L CO.,LTD

MS-7313

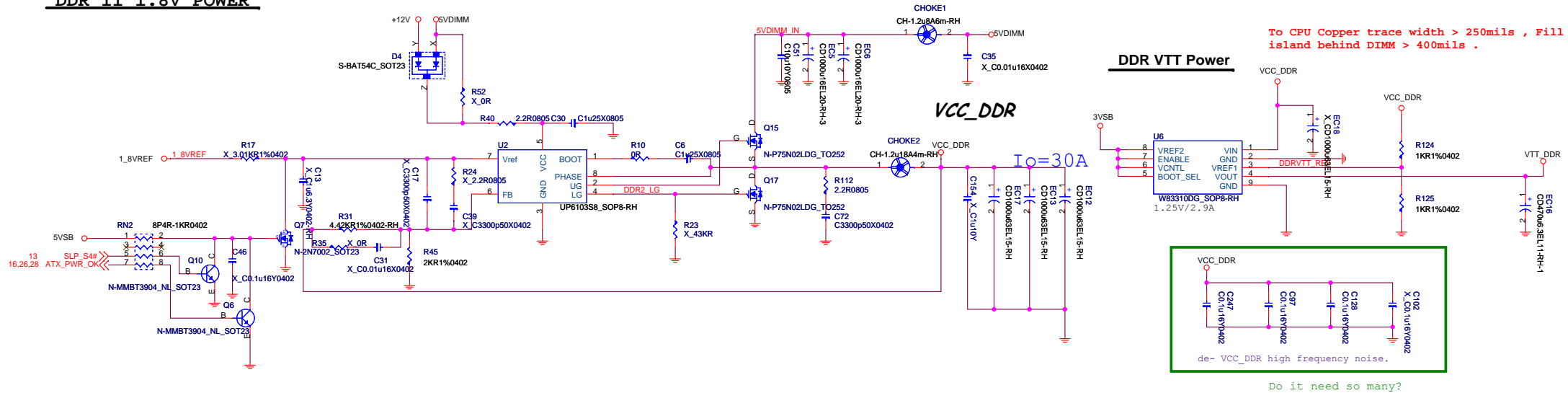
Size Custom	Document Description VGA Connector	Rev 1.0
Date: Tuesday, December 18, 2007		Sheet 27 of 33



VTT_SEL = L	V_FSB_VTT=1.1V	For future KENTSFIELD processor. (FSB1333, Quad-Core)
VTT_SEL = H	V_FSB_VTT=1.2V	For normal processors.

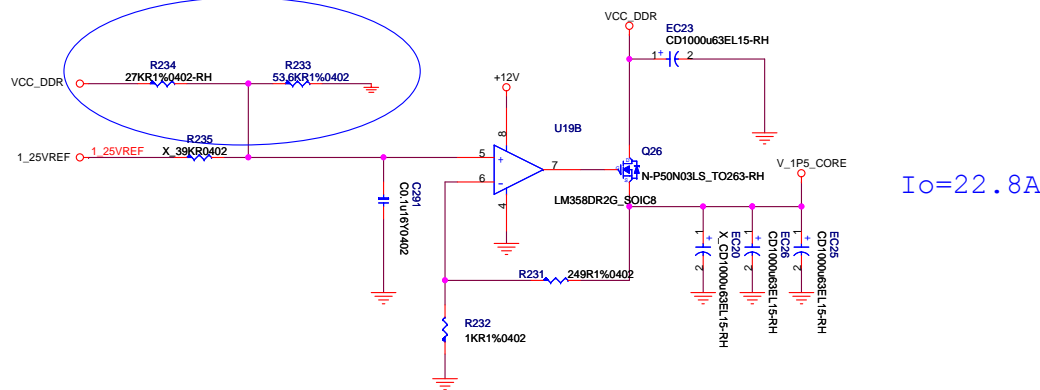


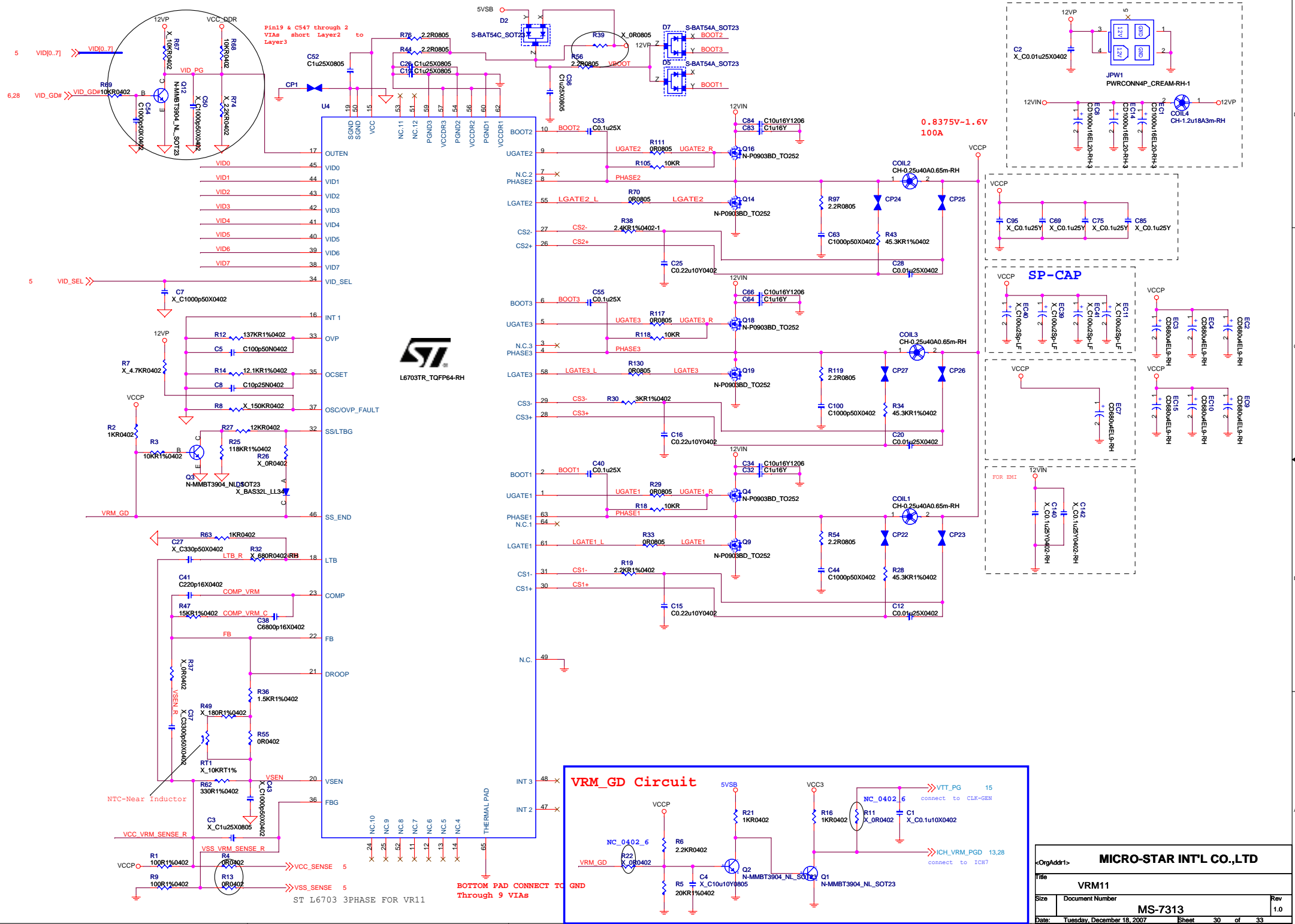
DDR II 1.8V POWER



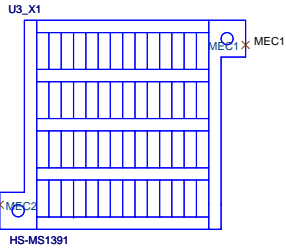
1.5V Core

For cost down

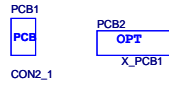
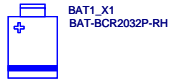
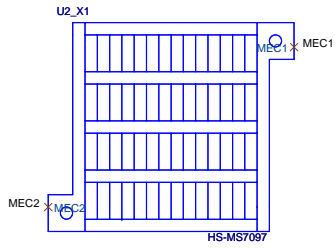




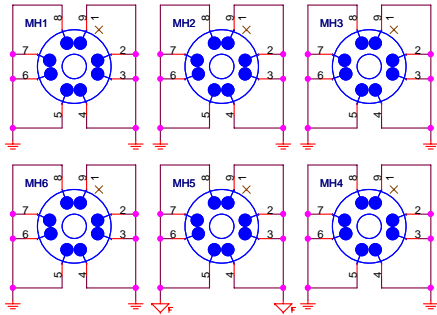
ICH7 HEATSINK



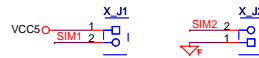
MCH HEATSINK



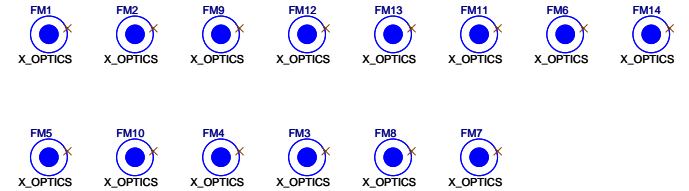
Mounting Holes



Simulation



Optics Orientation Holes



ICH7									
GPIO	Alt Func	PIN	I/O/NC	POWER	PU	SMI	TOL	DEFAULT	SIGNAL NAME
GPIO0	Unmultiplexed	AB18	I/O	CORE	N	Y	3.3V	GPI	GPIO3(pull high)
GPIO1	REQ5#	C8	I/O	CORE	N	Y	5V	GPI	PREQ#5
GPIO2	PIRQE#	G8	I/OD	CORE	N	Y	5V	GPI	GPIO2(pull high)
GPIO3	PIRQF#	F7	I/OD	CORE	N	Y	5V	GPI	GPIO3(pull high)
GPIO4	PIRQG#	F8	I/OD	CORE	N	Y	5V	GPI	GPIO4(pull high)
GPIO5	PIRQH#	G7	I/OD	CORE	N	Y	5V	GPI	GPIO5(pull high)
GPIO6	Unmultiplexed	AC21	I/O	CORE	N	Y	3.3V	GPI	ATADET0
GPIO7	Unmultiplexed	AC18	I/O	CORE	N	Y	3.3V	GPI	STRAPPED HI
GPIO8	Unmultiplexed	E21	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO9	Unmultiplexed	E20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO10	Unmultiplexed	A20	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO11	SMBALERT#	B23	I/O	Resume	N	Y	3.3V	Native	STRAPPED HI
GPIO12	Unmultiplexed	F19	I/O	Resume	N	Y	3.3V	GPI	SIO_PME#
GPIO13	Unmultiplexed	E19	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO14	Unmultiplexed	R4	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO15	Unmultiplexed	E22	I/O	Resume	N	Y	3.3V	GPI	STRAPPED HI
GPIO16	Unmultiplexed	AC22	I/O	CORE	N	N	3.3V	GPO	NC
GPIO17	GNT5#	D8	I/O	CORE	N	N	3.3V	GPO	STRAPPED L
GPIO18	Unmultiplexed	AC20	I/O	CORE	N	N	3.3V	GPO	NC
GPIO19	SATA_1GP	AH18	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO20	Unmultiplexed	AF21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO21	SATA_0GP	AF19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO22	REQ4#	A13	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO23	LDRQ_1#	AA5	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO24	Unmultiplexed	R3	I/O	Resume	N	N	3.3V	GPO	NC
GPIO25	Unmultiplexed	D20	I/O	Resume	Y	N	3.3V	GPO	GPIO25(high 7507,low 7398)
GPIO26	Unmultiplexed	A21	I/O	Resume	N	N	3.3V	GPO	USB_EN
GPIO27	Unmultiplexed	B21	I/O	Resume	N	N	3.3V	GPO	NC
GPIO28	Unmultiplexed	E23	I/O	Resume	N	N	3.3V	GPO	NC
GPIO29	OC5#	C3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#2
GPIO30	OC6#	A2	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO31	OC7#	B3	I/O	Resume	N	N	3.3V	GPI	USB_OCP#3
GPIO32	Unmultiplexed	AG18	I/O	CORE	N	N	3.3V	GPO	BIOS_WP#(fill with 1)
GPIO33	Unmultiplexed	AC19	I/O	CORE	N	N	3.3V	GPO	NC
GPIO34	Unmultiplexed	U2	I/O	CORE	N	N	3.3V	GPO	NC
GPIO35	SATACLKREQ#	AD21	I/O	CORE	N	N	3.3V	GPO	NC
GPIO36	SATA2GP	AH19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO37	SATA3GP	AE19	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO38	Unmultiplexed	AD20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO39	Unmultiplexed	AE20	I/O	CORE	N	N	3.3V	GPI	STRAPPED HI
GPIO48	GNT4#	A14	I/O	CORE	N	N	3.3V	Native	STRAPPED HI
GPIO49	CPUPWRGD	AG24	I/O	V_CPU_IO	N	N	V_CPU_IO	Native	H_PWRGD
Following are the GPIOs that need to be terminated properly if not used: GPIO[39:36,23:21,19,7:0]: default as inputs and should be pulled up to Vcc3_3 if unused. GPIO[31:29,15:8]: default as inputs and should be pulled up to VccSus3_3 if unused.									

SIO Fintek71882FG(CONTINUE)					
GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO0	VIDOUT0	49	MCH_BSEL0	O12	
GPIO1	VIDOUT1	50	MCH_BSEL1	O12	
GPIO2	VIDOUT2	51	MCH_BSEL2	O12	
GPIO3	VIDOUT3	52	NC	O12	
GPIO4	VIDOUT4	53	NC	O12	
GPIO5	VIDOUT5/SIC	54	NC	I/OD12t	
GPIO6	SLOT0CC#	55	GPO	I/OD12t	
GPIO7	Turbo1#/WDTRST#	56	WDTRST#	OD12-5v	
GPIO15	LED_VSB/ALERT#	64	LED_VSB	OD12	
GPIO16	LED_VCC/Turbo2#	65	LED_VCC	OD12	
GPIO20	PCIRST1#	74	PCIRST1#	OD12	
GPIO21	PCIRST2#	75	PCIRST2#	O12	
GPIO22	PCIRST3#	76	PCIRST3#	O12	
GPIO23	RSTCON#	77	RSTCON#	OD12	
GPIO24	ATXPG_IN	78	ATXPG_IN	AIN	
GPIO32	PWROK	84	PWROK	OD12	
GPIO26	PWSIN#	80	PWSIN#	INts5v	
GPIO27	PWSOUT#	80	PWSOUT#	OD12	
GPIO30	S3#	82		INts5v	
GPIO31	PSON#	83	PSON#	OD12-5v	
GPIO33	RSMRST#	85	RSMRST#	OD12	
GPIO40	FANIN3	25	FANIN3	INts5v	
GPIO41	FAN_CTL3	26	FAN_CTL3(NC)	OD12-5v	
GPIO25	PME#	79	PME#	OD12-5v	
GPIO10	SPI_SLK/FANIN4	59	GPIO10(NC)	I/OD12t	
GPIO11	SPI_CS0#/FANCTL4	60	GPIO11(NC)	I/OD12t	
GPIO12	SPI_MISO/FANCTL1_1	61	GPIO12(NC)	I/OD12t	
GPIO13	SPI_MOSI/BEEP	62	BEEP(NC)	OD24	
GPIO14	FWH_DIS/WDTRST#/SPI_CS1#	63	GPIO14	I/OD12t	
GPIO42	IRTX	27	IRTX	O12	
GPIO43	IRRX	28	IRRX	INts	
GPIO17		66	NC	I/OD12t	

PCI Config.

DEVICES		MCP1 INT	PIN REQ#/GNT#	IDSEL	CLOCK
PCI1	PIRQ#A	PREQ#0 PGNT#0	AD16	PCI_CLK0	
	PIRQ#B				
	PIRQ#C				
	PIRQ#D				
PCI2	PIRQ#B	PREQ#1 PGNT#1	AD17	PCI_CLK1	
	PIRQ#C				
	PIRQ#D				
	PIRQ#A				

DDRII DIMM Config.

DEVICE	ADDRESS	CLOCK
DIMM A	A0H	P_DDR0_A/N_DDR0_A
		P_DDR1_A/N_DDR1_A
		P_DDR2_A/N_DDR2_A
		P_DDR0_B/N_DDR0_B
DIMM B	A4H	P_DDR1_B/N_DDR1_B
		P_DDR2_B/N_DDR2_B

JUMPER SETTING

JBAT1	(1-2)NORMAL	(2-3)CLEAR
--------------	--------------------	-------------------

File BIOS Request Form		
Size C	Document Number MS-7313	Rev 1.0
Date:	Monday, December 10, 2007	Sheet 32 of 33

0A Change list:

- 1.Remove 1394 & PCIE-X1;
- 2.modify usb1
- 3.Remove EC18,EC19,EC57,EC62,D19, D22, D24, D25; R87,R91,R92,R96
- 4.5VREF Change 5817 to 3904
- 6.Change DDR Chock to 8A, 18A
- 7.LAN的EEPROM部分: R201,U29,R213不上件;
- 8.合并LED_VCC,LED_VSB两个信号电阻为排阻; ICH_VRM_PGD;ATX_PWR_OK两个信号电阻为排阻
- 9.Modify page NO. and off page ;
- 10.Change EC64,EC65,EC88 TO MLCC C76 , C77 , C85
- 11.Change audio 6 Port to 3 Port
- 12.power circuit update :R372 上件, RT3 & R244不上件
- 13.remove D52 , change C278 to 0805 10U
- 14.For EMI Request:remove C91 ,ADD 2 pcs VCC_DDR-VTT_DDR 0.1uf cap : C262 C266 ;
ADD CTRL18-GND 0.1ufcap: C221 , AVDD33-GND 0.1uf cap:C230 , AVDD18-GND 0.1ufcap: C219
- 15.Modify LPT:remove D7,D8 ;change 8P4R to 10P8R RN74,RN75;
- 16.Modify PCI RN39,RN40 8P4R to RN76 10P8R AND remove c148, c187 for EMI;
- 17.统一 USB CONNECTOR netname

For CostDown

- 18.Delet: EC33,EC35 (VCC5) for USB power;EC31 for 3VSB power;EC45 for 5VCC power;EC49,EC89 for 3VCC power
- 19.Delet EC68 (VCCP) for power team ; Change H/L-mos to D03-0903BDB-N03 H-MOS, D03-75N022B-N03 L-MOS
- 20.Change EC40 to C616(1206) ; C608,C609 change to 1206
- 21.Change Q17 TO252 to SOT_89
- 22.Remove C206,C267,C238,RN16 ,R265,R266,C138; Change C237,C601 22uf to 10uf;
Remove R118,R119 USE RN31; Remove R384,R388,R389 USE RN77;
- 23.Change R215 0805 to 0603 ,Remove C269, R226 ,R75; Change L-mos D03-75N022B-N03 to D03-0903BDB-N03;
Remove R163,RT1,Stuff Q19 for system Tem;
RemoveC173,C224,C56,C57,C58
- 24.Delet Q26,R393,R202,Q42,R343,C277,R168,Q43,C276,C276,D19,R435,R161
- 25.Remove U9,U10,And stuff R479,R480 for VGA; Remove C189,C200,C271
- 26.Swap JUSB1 PIN and LPT PIN ,Delet EC12 for Power Team,Delet c224 C186;
Delet R400 R403 R406 change to line,Delet R335 C266 D28 CP34 C229 C345 C465 C109 C148 CP48 C43 CP27 CP28
- 27.Dealet CP32 CP46 For EMI ,Rename ,Delet C23 for power team ,Change R171 0603 to 0402
- 28.Change PGND to GND For EMI
- 28.Change X_J2 GND to GNDF For LAYOUT

Title			
History			
Size	Document Number		Rev
Custom	MS-7313		1.0
Date:	Monday, December 10, 2007	Sheet	33 of 33